POWER REDUCTION CIRCUIT AND METHOD WITH MULTI CLOCK BRANCH CONTROL

Abstract Of The Invention

A power consumption reduction circuit and method utilizes a memory clock source and a memory clock divider circuit that generates divided memory clock output signals as a plurality of corresponding independent clock signals to a number of different processing engines. A memory clock divider circuit and method selectively activates a plurality of independent clock signals in response to received condition data. In one embodiment, an engine clock source is also coupled through a switching circuit such that it is selectively output to one or more processing engines. The switching circuit disables the output from the engine clock based on register condition data. In another embodiment, a plurality of memory read latch circuits are controlled by a memory read latch control circuit. The memory read latch control circuit is operative to dynamically activate and deactivate the plurality of memory read latches based on detected memory read requests to facilitate memory access activity-based power reduction